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Semiconductor Manufacturing, IEEE Transactions on , Volume: 16

Issue: 2 , May 2003

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[\[Abstract\]](#)[\[PDF Full-Text \(702 KB\)\]](#) **IEEE JNL****2 Effective safety property checking using simulation-based sequential ATPG***Shuo Sheng; Takayama, K.; Hsiao, M.S.;*

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June 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(763 KB\)\]](#) **IEEE CNF****3 RTL level preparation of high-quality/low-energy/low-power BIST***Santos, M.B.; Teixeira, I.C.; Teixeira, J.P.; Manich, S.; Rodriguez, R.; Figueras, J.;*

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4 Cu/LKD-5109 damascene integration demonstration using**FF-02 low-k spin-on hard-mask and embedded etch-stop**

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Harvey, M.C.; Lott, J.A.; Nelson, T.R., Jr.; Stintz, A.; Malloy, K.J.;
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D. W. Hightower , B. A. Unger

Proceedings of the ninth design automation workshop on Design automation June 1972

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Chad D. DeJong , Seth A. Fischbein

Proceedings of the 32nd conference on Winter simulation December 2000

Semiconductor fabrication facilities (fabs) continue to expand in both complexity and volume. As a result, integrated models are required to determine even high level impacts to key success indicators. In order to gain insight into how the components of a factory impact performance metrics, Intel uses an integrated discrete-event simulation modeling approach. Two models, one fab capacity and one automation model, are used. This paper discusses the methodology for building and integrating both mo ...

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